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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/486,582
Filing Date: July 10, 2000
Appellant(s): GEORGE ET AL.

Timothy L. Boller
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06 September 2007 appealing from the Office action mailed 08 February 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Uramoto, S. "DCT/IDCT Processor and data processing method" European Patent Application 0 506 111 A2 27 March 1992

"Information technology -- Coding of moving pictures and associated audio for digital storage media at up to about 1,5 Mbit/s -- Part 3: Audio" ISO Standard 11172-3, 01 August 1993

"Discrete Cosine Transform" Wikipedia.com overview entry retrieved 27 November 2007

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1 – 20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1 – 10, 18, 19 and 20 are directed to a method for decoding digital audio signals. The method, therefore, falls into one of the four enumerated statutory categories (i.e. a process). However, the claim, when considered as a whole covers the judicial exception of a mathematical algorithm. The claims involve various calculations and manipulations of digital audio data. These calculations are nothing more than a mathematical algorithm.

Next, it must be determined whether there is a practical application by physical transformation or a practical application that produces a useful, tangible and concrete result.

There is no practical application by physical transformation present in the claims. Digital audio data is not physical, rather a form of energy representing data. Manipulating this energy does not involve a physical transformation.

Lastly there is no practical application by the production of a useful, tangible and concrete result. Examining the claim as a whole, the final result achieved is forming decoded audio signals from two sequences of values. This is not a useful, tangible and concrete result, but rather the result of the process.

Claims 11 – 17 are means plus function, thus one must examine the specification to determine the means. The first stem is means for receiving. On page 5 of the specification, an MPEG audio decoder circuit 20 for receiving a bitstream. This decoder is presumably a typical MPEG audio decoder as is further evidenced in lines 20 – 25 of page 5. The preprocessing means is further described on page 7 involving pre-computing the sum and difference of the sample data in a computational loop which is done on a general purpose DSP. The transform output means are the general output means of the device. The various means for implementing the MPEG decoder are described as a DSP general processor. Thus the claims as a whole are nothing more than a program or steps performed on a general purpose processor. The code/program

implemented on the processor does not fall within one of the four enumerated statutory categories.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 6, 11, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uramoto (European Patent Application 0 506 111 A2).

Regarding **Claims 1 and 11**, Uramoto discloses:

A method of decoding digital data (entire document), comprising the steps of:

-obtaining an input sequence of data elements (i.e. intermediate terms) representing encoded samples (Fig. 11 element 3 outputs intermediate terms which are then input to post processing section 7; page 12 lines 10 - 15);

preprocessing the input sequence of data elements by calculating an array of sum data and an array of difference data using selected data elements from the input sequence (i.e. post processing section 7 has the same configuration of as that of Fig. 5; the input circuit of Fig. 5, element 21 sequentially or alternately receives the

intermediate terms to apply a desired combination of the terms to the add/subractors 22 and 23; the data Mi and Ni is sequentially added and subtracted as taught in on page 8 lines 25 – 32; see also page 12 lines 17 - 28);

producing a first sequence of output values using the array of sum data (i.e. the adder 22 of post processing section 7 outputs sum data as taught on page 8 lines 29 – 30 see also page 12 lines 17 - 28);

producing a second sequence of output values using the array of difference data (i.e. the subtactor 23 of post processing section 7 outputs difference data as taught on page 8 line 31 see also page 12 lines 17 - 28);

forming decoded signals from the first and second sequences of output values (i.e. the output of the post processing section).

Uramoto does not disclose that the input sequence represents encoded digital audio data. However, Uramoto discloses that the intermediate values are derived from digital video data; page 2. Using Uramoto to operate on digital audio data in place of digital video data would have been obvious at the time of the invention. One would have been motivated to do so in order to process audio data at a high speed; page 2 of Uramoto.

Regarding **Claim 2**, in addition to the elements stated above regarding claim 1, Uramoto further discloses:

wherein the array of sum data is obtained by adding together respective first and second data elements from the input sequence, the first and second data elements

being selected from mutually exclusive sub-sequences of the input sequence (page 12 line 20; and page 8 lines 27 – 29).

Regarding **Claim 3**, in addition to the elements stated above regarding claim 1, Uramoto further discloses:

wherein the array of difference data is obtained by subtracting respective first data elements from corresponding second data elements of the input sequence, the first and second data elements being selected from mutually exclusive subsequences of the input sequence (page 12 line 23; and page 8 lines 27 – 31).

Regarding **Claim 4**, in addition to the elements stated above regarding claim 1, Uramoto further discloses:

wherein the step of preprocessing the input sequence of data elements to produce an array of sum data and an array of difference data comprises dividing the input data sequence into first and second equal sized sub-sequences (page 12 lines 20 and 23), the first sub-sequence comprising the higher order data elements (page 12 line 23) of the input sequence and the second sub-sequence comprising the low order data elements of the input sequence (page 12 line 20) (also see page 8 lines 27 – 31);

producing the array of sum data by adding together each respective data element of the first subsequence with a respective corresponding data element of the second sub-sequence (i.e. elements form Mi are added to elements of Ni and the difference is calculated as well; page 12 lines 20 – 23 and page 8 lines 27 – 31)

and producing the array of difference data by subtracting each respective data element of the first sub-sequence from a respective corresponding data element of the second sub-sequence (i.e. elements form Mi are added to elements of Ni and the difference is calculated as well; page 12 lines 20 – 23 and page 8 lines 27 – 31).

Regarding **Claim 5**, in addition to the elements stated above regarding claim 1, Uramoto further discloses:

wherein the step of calculating a first sequence of output values comprises performing a multiply-accumulate operation utilizing each of the sum data elements (i.e. the output of the addition and subtraction (fig. 5 element 500) is applied to a data rearranging circuit which supplies an output (fig 7A elements 500 and 501), this output is then applied to a product sum operation circuit (fig. 8 element 501))

Regarding **Claim 6**, in addition to the elements stated above regarding claim 1, Uramoto further discloses:

wherein the step of calculating a second sequence of output values comprises performing a multiply-accumulate operation utilizing each of the difference data elements (i.e. the output of the addition and subtraction (fig. 5 element 500) is applied to a data rearranging circuit which supplies an output (fig 7A elements 500 and 501), this output is then applied to a product sum operation circuit (fig. 8 element 501).

Regarding **Claim 18**, in addition to the elements stated above regarding claim 2, Uramoto further discloses:

wherein the array of difference data is obtained by subtracting respective first data elements from corresponding second data elements of the input sequence, the first and second data elements being selected from mutually exclusive subsequences of the input sequence (i.e. the subtactor selects the set of x0 and x7 to create a difference value from the sets of data of (x0, x7), (x1, x6), (x2, x5) and (x3, x4); sequences Mi and Ni in the post processing section as taught on page 12).

Regarding **Claim 19**, in addition to the elements stated above regarding claim 1, the output of the addition and subtraction (fig. 5 element 500) is applied to a data rearranging circuit which supplies an output (fig 7A elements 500 and 501), this output is then applied to a product sum operation circuit (fig. 8 element 501) (i.e. wherein the step of producing a first sequence of output values comprises performing a multiply-accumulate operation utilizing each of the sum data elements).

Claims 7 – 10 and 12 – 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uramoto (European Patent Application 0 506 111 A2) in view of ISO Standard 11172-3.

Regarding **Claim 7**, in addition to the elements stated above regarding claim 1, Uramoto does not disclose the limitations of claim 7.

ISO discloses wherein the input sequence of data elements is derived from MPEG encoded audio data (page 41 and title), and wherein the decoded audio signals comprise pulse code modulation samples (i.e. the audio data left and righ channel outputs; page 41).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the samples of the combination in ISO's decoder. One would have been motivated to do so to make the audio decoding system of the modified Uramoto system compatible with a commonly available audio encoding standard such as the MPEG standard.

Regarding **Claim 8**, Uramoto discloses adder 22 adds the data i.e. (x0 + x7) (page 8 lines 27 – 29) and subtractor 23 subtracts the data (x0 – x7) (page 8 lines 27 – 31); which in a) calculating an array of sum data $S_{ADD}[k]$ according to

$$S_{ADD}[k] = S[k] + S[m-1-k] \qquad \text{for } k = 0, 1, \ldots(m/2-1)$$

b) calculating an array of difference data $S_{SUB}[k]$ according to

$$S_{SUB}[k] = S[k] - S[m-1-k] \qquad \text{for } k = 0, 1, \ldots(m/2-1)$$

Uramoto does not disclose the rest of the claimed limitations in claim 8. ISO discloses an inverse modified discrete cosine transform (page 36). ISO also discloses multiplying samples by this function (page 41) i.e.

c) calculating a first output audio data sample by a multiply-accumulate operation according to

$$V[2i] = V[2i] + N[i, k]*S_{ADD}[k] \qquad \text{for } k = 0, 1, \ldots (m/2-1)$$

$$\text{where } N[i, k] = \cos\left[\frac{(32+2i)(2k+1)\pi}{64}\right]$$

d) calculating a second output audio data sample by a multiply-accumulate operation according to

$$V[2i+1] = V[2i+1] + N[i, k]*S_{SUB}[k] \qquad \text{for } k = 0, 1, \ldots (m/2-1)$$

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the samples of the combination in ISO's decoder. One would have been motivated to do so to make the audio decoding system of the modified Uramoto system compatible with a commonly available audio encoding standard such as the MPEG standard.

Regarding **Claim 9**, in addition to the elements stated above regarding claim 8, ISO discloses any number of samples from 12 – 36 (page 36).

Regarding **Claim 10**, in addition to the elements stated above regarding claim 8 ISO discloses decoding MPEG audio (page 41 and title).

Regarding **Claim 12**, in addition to the elements stated above regarding claim 11, Uramoto does not explicitly disclose the elements set forth in claim 12.

ISO discloses the use of the inverse modified discrete cosine transform to decode audio data (pages 36 and 41) which meets the limitations.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the samples of the combination in ISO's decoder. One would have

been motivated to do so to make the audio decoding system of the modified Uramoto system compatible with a commonly available audio encoding standard such as the MPEG standard.

Regarding **Claim 13**, in addition to the elements stated above regarding claim 12, ISO discloses decoding MPEG audio (page 41 and title).

Regarding **Claim 14**, claim 14 is rejected under the same grounds as claims 1, 11, 12 and 13 as stated above.

Regarding **Claim 15**, in addition to the elements stated above regarding claim 14, ISO discloses wherein the means for receiving an input sequence comprises a bitsgream unpacking and decoding circuit (page 41).

Regarding **Claim 16**, in addition to the elements stated above regarding claim 14, the combination further discloses:

wherein the means for producing an array of sum data and an array of difference data comprises a reconstruction circuit (i.e. the sum and difference operations are part of a processing circuit; pages 8 and 12; page 12 and Fig. 11).

Regarding **Claim 17**, in addition to the elements stated above regarding claim 14, Uramoto further discloses:

wherein the means for producing a first sequence of decoded output values comprises an inverse mapping circuit (i.e. the output circuit outputs the addition and subtraction data; page 12 and Fig. 11).

Regarding **Claim 20**, in addition to the elements stated above regarding claim 9, wherein the steps of decoding are repeated for decoding a series of frames of encoded audio data in an MPEG format (i.e. the bit stream inputs a series of MPEG frames to be decoded; page 41).

(10) Response to Argument

In section A (1), Appellant argues that claims 1-7, 18 and 19 are directed to statutory subject matter. Appellant contends that the transformation of data elements are a physical transformation and the audio output is a useful tangible and concrete result.

The Examiner made a 101 rejection of claims 1-7, 18 and 19 under the bases that they were nothing more than a mathematical algorithm. Next, the Examiner argued that the claims did not claim a physical transformation nor a useful, tangible and concrete output. Examiner contends that the alleged "physical transformation" of the manipulation of data elements is not a physical transformation as required. Again, it is submitted that is nothing more than a transformation of energy, and not a physical transformation. Next, Appellant argues that the claim is directed to forming a decoded

audio signal produces a useful tangible and concrete result. However, when viewing the claim as a whole, this is just another step in the mathematical algorithm. There is no indication that this signal is output or what is done with it at the next step. It is merely just calculated and left for the next step.

Finally it should be noted that these claims do not require any type of machine, such as a computer. Thus, the methods appear to be disembodied concepts or abstractions. This abstraction is in the form of a mathematical algorithm. While it may not seem like an algorithm in claim 1, a brief review of claim 8 clearly shows that each of the steps in claim one are directed to a calculation.

In **section A (2)**, Appellant argues that claims 8-10 and 20 are directed to statutory subject matter for the same reasons as above in A (1). Examiner contends these claims are non statutory for the same reasons stated in A (1).

In **section A (3)**, Appellant argues that claims 11-13 are directed to statutory subject matter. Appellant contends that these claims are statutory because "The use of mathematical formulae or relationships to describe the electronic structure an operation of an apparatus does not make it non-statutory." Further, specific software and hardware combinations are described in the specification for performing the recited functions.

First, a general purpose machine which merely performs an algorithm has been held nonstatutory as an attempt to patent the algorithm itself, see In re de Castelet, 562 F.2d 1236, 1243, 195 USPQ 439, 445 (CC PA 1977).

Secondly, these claims are means plus function claims, which per 112 6th paragraph, one must look in the specification to determine exactly what these means cover. This process is clearly described as a program loop on page 7 as well as through the figures. These flowcharts indicate nothing more than software. Further, even if they ***may*** performed on a processor it is not necessarily required and thus can be interpreted as nothing more than program code. Computer programs ***do not fall within one of the four statutory categories***.

In **section A (4)**, Appellant argues that claims 14-17 are directed to statutory subject matter for the same reasons as above in A (3). Examiner contends these claims are non statutory for the same reasons stated in A (3).

In **section B**, Appellant argues that the Examiner has failed to establish a prima facie case of obviousness. Appellant then states various requirements for a 103 rejection. Appellant has not stated which requirements have not been met or given any reasoning why a prima facie case of obviousness has not been made. Rather, Appellant merely states that one is not made.

For clarification, Examiner will show that all three requirements were met and give further evidence for the modification of Uramoto.

Requirement 1, "show some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or combine the reference teachings." This is clearly shown in the final rejection on page 7, which states "one would have been motivated to do so [i.e. use the decoder for audio instead of video] in order to process audio data at a high speed; page 2 of Uramoto." Furthermore, the knowledge of substitution of audio in place of video in various encoders or decoders is notoriously well known in the art. The discrete cosine transform (DCT) is notoriously well known in the art to aid in compression of various media such as audio, images and video. In the wikipedia.com entry for "Discrete Cosine Transform," it is shown that DCT is useful for audio compression under the "Informal Overview" and "Computation" sections. Because Uramoto is using a DCT, it would have been clear to one of ordinary skill in the art to modify it to process audio, as Uramoto discloses that you can process the data at a high rate of speed.

Requirement 2, "there must be a reasonable expectation of success." Since the DCT has been clearly shown to be useful for audio and video, it is clear to one of ordinary skill in the art that there would be a reasonable expectation of success.

Requirement 3, "the prior art reference (or combined references) must teach or suggest all the claim limitations. These limitations are clearly shown in the final rejection.

In **section 1**, Appellant contends that claims 1-6, 11, 18 and 19 are not obvious over Uramoto.

Appellant first states: "The portions of Uramoto to which the Examiner points do not teach or suggest a method of decoding digital audio data, as recited. To the extent decoding is addressed, a different method is taught. The portion of Uramoto to which the Examiner points, including the discussion of digital video encoding on page 2, teaches using the discrete cosine transform (DCT) for encoding. See Figure 5 of Uramoto and the accompanying description thereof on page 8, lines 15-37."

Examiner partially agrees with Appellants statements. However, an incomplete review of Uramoto would lead one to believe that the rejection relies upon the encoder stage. It is clearly shown in Uramoto that the same exact structure is used for the decoding stage. Figure 11 is the decoding stage, i.e. the inverse discrete cosine transform. Uramoto clearly states that element 7 of figure 11 has the same structure as figures 5 and 6 (page 12 of Uramoto). Thus, while figure 5 is used in the rejection to point out specific structure, it is actually the post processor of figure 11 (the decoder) which is relied upon for the rejection. Further Appellant points this out at the bottom of page 11 of the arguments.

Next Appellant states "Contrary to the Examiner's position, the intermediate data is not "an input of sequence of data elements representing encoded audio samples." It is unclear to the Examiner as to how Appellant arrives at this allegation as there are no rationale present. Appellant appears to just state that the intermediate data cannot be

the input data. Since there is no rationale present, further clarification will be given to the rejection. The limitation in question reads "obtaining an input sequence of data elements representing encoded audio samples." Post processing section 7 clearly receives an input sequence of data elements, the intermediate terms. These intermediate terms represent encoded video data (video decoder receiving video data). In the rejection, it was put forth that it would have been obvious to substitute audio data for video data.

As such, the post processing section "obtains an input sequence of data elements" (i.e. the intermediate terms are input to the post processing section, shown in Fig. 11 and page 12) "representing encoded audio samples" (i.e. encoded video samples represented by intermediate terms in Uramoto modified to be audio samples by the obviousness rejection).

Without any rationale, it is unclear why Appellant states this intermediate data cannot read upon the input sequence as it is "input" to the post processing section and represents encoded video (audio in the obvious rejection) data.

The remaining arguments in Section 1 are based upon the same allegation that the intermediate terms are operated on and not the input sequence. These allegations cannot stand for the same reasons as stated above.

In **section 2**, Appellant argues that claims 7, 12 and 13 are not obvious over Uramoto in view of ISO Standard 11172-3 for the same reasons as above in section 1.

Examiner contends these arguments cannot stand for the same reasons stated in section 1.

Additionally, Appellant states: "Further, one would not be motivated to combine the inverse modified discrete cosine transform (IMDCT) with Uramoto, which as discussed above teaches the DCT for encoding and IDCT for decoding. Accordingly, claims 7, 12 and 13 are not rendered obvious by Uramoto, alone or in combination with ISO Standard 11172-3."

However, again there is no rationale as to why one would not be motivated to combine these two references, merely a conclusory statement stating such. As shown in the rejection it would have been obvious to modify the system to be compatible with the MPEG standard. This is clearly desirable and notoriously well known in the art as the encoder can be used for audio as shown above, and making it compatible with a well known form of audio would be desirable.

In **section 3**, Appellant argues that claims 8-10 and 20 are not obvious over Uramoto in view of ISO Standard 11172-3 for the same reasons as above in sections 1 and 2. Examiner contends these arguments cannot stand for the same reasons stated in sections 1 and 2.

Additionally Appellant states: "Further, the sum output data xi = MI + Ni for I = 0, 1, 2, 3 and the difference output data xi = Mi - Ni for i = 4, 5, 6, 7 generated by post processing section 7 (Uramoto, page 12, lines 20-22 and Fig. 11) is not the same as the

array of sum data SADD[k] = S[k] + S[m-l-k] and the array of difference data Ssub[k] = S[k] - S(m-l-k) (for k = 0, 1 ...(rn/2- 1)), as claimed in claim 8."

Appellant rationalizes that these terms are comprised of additions and/or subtractions of products of input data and, by contrast, S[k] and S[m-1-k] are coded input digital audio samples. However, these intermediate terms are coded data. The have been manipulated but still represent encoded digital video data (audio data in the obviousness rejection) by nature that the original signal is an input video signal and while this signal may have been manipulated to reach these intermediate terms, the terms still represent encoded data.

In **section 4**, Appellant argues that claims 14-17 are not obvious over Uramoto in view of ISO Standard 11172-3 for the same reasons as above in sections 1,2 and 3. Examiner contends these arguments cannot stand for the same reasons stated in sections 1,2 and 3.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Andrew Flanders

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